REMARKS

In the Office Action dated July 14, 2005, the Examiner rejected claims 35, 37-39, 45, 47-49, 63 and 65-70. Reconsideration of the application in view of the amendments set forth above and the remarks set forth below is respectfully requested.

Rejection Under 35 U.S.C. § 102

In the Office Action, the Examiner rejected claims 35, 37, 45, 47, 63, 65, and 67 under 35 U.S.C. § 102(e) as being anticipated by Pai et al. (U.S. Patent No. 6,503,776 B2)("the Pai reference"). Specifically, with regard to the independent claims, the Examiner stated the following:

> Regarding claim 35. An integrated circuit comprising:
>
> a stack comprising at least two semiconductor die (130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20), each of the semiconductor die being coupled together by a first adhesive,, the first adhesive (166) being curable at a first temperature; and
>
> a substrate coupled (substrate 120 coupled to stack through chip 110 and adhesive 162) to one of the at least two semiconductor die by a second adhesive (112), the second adhesive being curable at a second temperature lower than the first temperature; (it is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight.
>
> Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a

product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two semiconductor die is functional (Pai teaches a dummy die, the dummy die serving a function, thus being functional.)

...

Regarding claim 45. An integrated circuit comprising a stack of at least two semiconductor die (130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20), each of the die being coupled to an adjacent die in the stack (110) by a respective layer of adhesive (162) prior to the stack being coupled to a packaging substrate. (The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two semiconductor die is functional (Pai teaches a dummy die, the dummy die serving a function, thus being functional.)

...

Regarding claim 63. An integrate circuit package comprising:

a substrate (120); and

a die stack coupled to the substrate (Figure 10), wherein the die stack comprises at least two semiconductor die (130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20), coupled together and wherein the dies stack is formed prior to being coupled to the substrate;

(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113)

wherein each die in the stack of at least two semiconductor die is functional (Pai teaches a dummy die, the dummy die serving a function, thus being functional.)

Office Action, pages 2-5.

Applicants respectfully traverse these rejections. Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under Section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

The present application relates generally to semiconductor processing. More particularly, it relates to an integrated circuit comprising a die stack coupled to a substrate. In summary,

independent claims 35, 45 and 63, as amended, each recite an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die, and "wherein each die in the stack of at least two semiconductor die is electrically functional." *See e.g.*, page 12, lines 10-12; page 17, line 13 – page 18, line 3. Further, claim 35 recites an integrated circuit comprising a die stack coupled to a substrate, "each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature," and wherein the stack is coupled to a substrate by a second adhesive, "the second adhesive being curable at a second temperature lower than the first temperature." *See e.g.*, page 12, lines 6-19; page 17, lines 10-13.

Applicants respectfully assert that the Pai reference fails to anticipate amended independent claims 35, 45, and 63. Specifically, as admitted by the Examiner on page 14 of the Office Action, the Pai reference fails to teach an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die, and "wherein each die in the stack of at least two semiconductor die is *electrically functional*," as recited in claims 35, 45, and 63. (Emphasis added). Indeed, in contrast to the present claims, the Pai reference discloses a die stack wherein a part of the stack includes a "dummy chip" with film adhesive that adheres to other die within the stack. Col. 3, line 65 – Col.4, line 5. The dummy chip is a die similar to the other die in the stack, but the dummy chip does not include wiring "because it is not employed in the device operation." Col. 3, lines 20-22. In other words, the dummy chip in the stack disclosed in the Pai reference is not electrically functional. Accordingly, the Pai reference fails to teach or

suggest a die stack wherein each of the die in the stack is electrically functional as recited in the present claims.

In view of the arguments set forth above, Applicants assert that independent claims 35, 45, and 63 are allowable over the prior art. Accordingly, Applicants request that the Examiner withdraw the rejection of claims 35, 45, 63, and the claims depending therefrom under 35 U.S.C. § 102. Further, Applicants request that the Examiner provide an indication of allowance for claims 35, 45, 63, and the claims depending therefrom.

In addition to the arguments set forth above, Applicants submit that the rejection of independent claim 35 is improper for an additional reason, as well. As set forth above, claim 35 additionally recites an integrated circuit comprising a die stack coupled to a substrate, "each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature," and wherein the stack is coupled to a substrate by a second adhesive, "the second adhesive being curable at a second temperature lower than the first temperature."

In rejecting claim 35, the Examiner stated:

> (it is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113)

Office Action, page 3.

While Applicants agree with the Examiner's statement regarding the patentable weight of process limitations in a product-by-process claim, Applicants respectfully traverse the Examiner's assertion that this claim is in fact a product-by-process claim. As stated above, claim 35 recites a first adhesive "being *curable* at a first temperature," and a second adhesive "being *curable* at a second temperature lower than the first temperature." (Emphasis added). The present claim does not recite an actual act of curing the adhesive. In contrast, the present claim recites physical qualities of each of the first and second adhesives. That is, the first adhesive is "curable at a first temperature," and the second adhesive is "curable at a second temperature." For instance, the first adhesive used in the die stack may have properties such that it is curable at a high temperature, such as in the range of 50-400° C, for example. Page 12, lines 8-9. The adhesive used to attach each die together may be different than the adhesive which may be used later to attach the die to the substrate. Page 12, lines 12-14. The second adhesive may be curable at a second temperature such as in the range of 50-100° C, for example. As will be appreciated by those skilled in the art, in order for the adhesives to be curable at different temperatures, the adhesives have different physical qualities. Accordingly, Applicants respectfully submit that these structural limitations should indeed be given patentable weight.

Applicants respectfully submit that the Examiner's failure to give patentable weight to these structural limitations was improper. For this additional reason, Applicants respectfully request that the Examiner withdraw the rejection and allow claim 35, as well as those claims dependent thereon.

Rejection Under 35 U.S.C. § 103

In the Office Action, the Examiner rejected claims 38, 39, 48, 49, and 66 under 35 U.S.C. § 103(a) as being unpatentable over the Pai reference in view of Huang et al. (U.S. Patent No. 6,753,206 B2)("the Huang reference"). Further, the Examiner rejected claims 68-70 under 35 U.S.C. § 103(a) as being unpatentable over the Pai reference in view of Hakey et al. (U.S. Patent No. 6,627,477 B1)("the Hakey reference").

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (P.T.O. Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (Bd. Pat. App. & Inter. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988). One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the

claimed invention. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). Moreover, the Examiner must provide *objective evidence*, rather than subjective belief and unknown authority, of the requisite motivation or suggestion to combine or modify the cited references. *In re Lee*, 61 U.S.P.Q.2d 1430 (Fed. Cir. 2002).

Rejection of Independent Claims 38, 48, and 66

Applicants respectfully assert that the cited references, taken alone or in combination, do not disclose or teach an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die and "wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack," as recited in claims 38, 48, and 66. As described in the present specification, Figs. 5C and 5D are cross-sectional views of "shingle stacks." Page 14, line 10. Shingle stacks are die stacks wherein upper die may overhang die below them in the stack such that their centers are not aligned. Page 14, lines 11-12. Contrary to the Examiner's assertion, the Huang reference does not disclose a shingle stack as reasonably interpreted in light of the present specification. That is to say that the Huang reference does not disclose a die stack wherein an upper die overhangs a lower die. Even if the integrated circuit package disclosed in the Huang reference could be fairly characterized as a die stack, the upper die *does not* overhang the die below. The upper die does not "overhang" anything. As clearly illustrated in Fig. 2 of the Huang reference, the upper die is adhered directly and completely to a lead frame. Thus, no portion of the upper die overhangs anything. Accordingly, neither of the cited references, either alone or in combination, discloses all of the features recited in claims 38, 48 and 66.

Further, Applicants respectfully submit that those skilled in the art would not be motivated to combine the Pai and Huang references, much less combine the references in the manner recited in the present claims. The Huang reference discloses a dual-chip integrated circuit package. "The dual-chip integrated circuit package includes a lead frame having a first set of leads and a second set of leads...in which the first integrated circuit chip is mounted on one side of the inner part of the first set of leads, and the second integrated circuit chip is mounted on the other side of the same..." Abstract. Accordingly, the Huang reference simply discloses coupling a first integrated circuit chip to the first side of a set of leads and coupling a second integrated circuit chip to the other side of a set of leads. As will be appreciated by those skilled in the art, lead frame technology is vastly different from technology related to packages incorporating a chip coupled to a substrate. Indeed, as discussed throughout the present specification, coupling a die or a die stack to a substrate may present certain challenges due to a mismatch in coefficients of thermal expansion of the die and the substrate. "The substrates on which the die are stacked generally have a different coefficient of thermal expansion." Page 3, lines 18-20. "Thus once the stack is formed on the substrate and cured as in typical die stacking systems, a mismatch in the coefficients of thermal expansion (CTEs) may be introduced, which may cause cracking or other problems with the die stack since the interface between each of the die and the interface between the die and the substrate are being cured at the same time but have different CTEs." Page 3, line 20 – page 4, line 1. Applicants provide this text as an example in support of the contention that those skilled in the art simply would not look to techniques for coupling die to lead frames, as in the Huang reference, to modify integrated circuit packages where die are attached to substrates as

in the Pai reference. Though the Huang reference does indeed illustrate a first functional die attached to one side of the lead frame and a second functional die attached to a second side of the lead frame, there is absolutely no motivation from this reference to stack two functional die together and then attach them to a substrate in the manner recited in the present application.

Further, Applicants are unaware of how one skilled in the art could modify the package disclosed in the Pai reference in view of the Huang reference to achieve the recited integrated circuit package. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (CCPA 1959); see M.P.E.P. § 2143.01. The Pai reference discusses perceived problems associated with multi-chip stacked packages including die attached directly to a substrate and stacked directly on top of each other. *See* Background. To solve problems such as bond line thickness and CTE mismatch, the Pai reference teaches introducing a dummy die (i.e., a die which is not electrically functional) between functional die. Though Applicants do not know how one would modify the integrated circuit package of Pai in view of the integrated circuit package of Huang, assuming *arguendo* that such a modification could be made, this would destroy the principle of operation taught by the Pai reference. That is, the Pai reference explicitly teaches inserting a dummy die between electrically functional die to create a consistent bond line. One skilled in the art would not be motivated to modify the Pai reference by removing the dummy die since it would destroy the principle of operation as taught by the Pai reference by

reintroducing the inconsistent bond line thickness and the problems associated with CTE mismatch.

Because the cited references, taken alone or in combination, fail to disclose each of the features recited in claims 38, 48 and 66, Applicants respectfully submit that the cited combination cannot possibly render the recited subject matter obvious. Further, as discussed in detail above, there is simply no suggestion to combine the cited references in the manner recited in the present claims. For this additional reason, Applicants again respectfully submit that the cited combination cannot possibly render the recited subject matter obvious. Thus, the Examiner's rejection of independent claims 38, 48 and 66, as well as those claims dependent thereon, is improper. Accordingly, Applicants respectfully request that the Examiner withdraw the rejection and provide an indication of allowance for claims 35, 48 and 66, as well as those claims dependent thereon.

In addition to the arguments set forth above, Applicants submit that the rejection of independent claim 38 is improper for an additional reason, as well. As set forth above, claim 38 additionally recites an integrated circuit comprising a die stack coupled to a substrate, "each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature," and wherein the stack is coupled to a substrate by a second adhesive, "the second adhesive being curable at a second temperature lower than the first temperature."

In rejecting claim 38, the Examiner stated:

> (It is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113)

Office Action, pages 6-7.

While Applicants agree with the Examiner's statement regarding the patentable weight of process limitations in a product-by-process claim, Applicants respectfully traverse the Examiner's assertion that this claim is in fact a product-by-process claim. As stated above, claim 38 recites a first adhesive "being *curable* at a first temperature," and a second adhesive "being *curable* at a second temperature lower than the first temperature." (Emphasis added). The present claim does not recite an actual act of curing the adhesive. In contrast, the present claim recites physical qualities of each of the first and second adhesives. That is, the first adhesive is "curable at a first temperature," and the second adhesive is "curable at a second temperature." For instance, the first adhesive used in the die stack may have properties such that it is curable at a high temperature, such as in the range of 50-400° C, for example. Page 12, lines 8-9. The adhesive used to attach each die together may be different than the adhesive which may be used later to attach the die to the substrate. Page 12, lines 12-14. The second adhesive may be curable at a second temperature such as in the range of 50-100° C, for example. As will be appreciated by those skilled in the art, in order for the adhesives to be curable at different temperatures, the adhesives have different physical qualities. Accordingly, Applicants respectfully submit that these structural limitations should indeed be given patentable weight.

Applicants respectfully submit that the Examiner's failure to give patentable weight to these structural limitations was improper. For this additional reason, Applicants respectfully request that the Examiner withdraw the rejection and allow claim 38, as well as those claims dependent thereon.

Rejection of Independent Claims 68, 69, and 70

Applicants respectfully assert that the cited references, taken alone or in combination, do not disclose or teach an integrated circuit comprising a stack coupled to a substrate, wherein the stack comprises at least two semiconductor die and "wherein each die in the stack of at least two die is successively thinner than the previous die," as recited in claims 68, 69, and 70. The Hakey reference merely discloses a method of achieving coplanarity between chips. Col. 4, lines 62-63; Fig. 6. While it is true that the Hakey reference discloses chips 12 of the varying thicknesses in the Z-axis, these chips are attached directly to a substrate 10. *See* Fig. 3. That is to say, each of the chips 12 are positioned directly adjacent to one another, not on top of one another. Applicants respectfully submit that there is absolutely no motivation provided in either the Pai reference or the Hakey reference that would suggest using the die of varying thickness as provided in the direct mount package disclosed in the Hakey reference with the die stack of the Pai reference.

As repeatedly discussed throughout the Hakey reference, the reference is directed specifically to aligning the chips 12 adjacent to one another such that the active surface of the devices are co-planar. *See e.g.* Abstract; Fig. 6. Because the Hakey reference is directed to

ensuring that each of the active surfaces on the chips 12 are co-planar, the reference actually teaches away from forming a die stack. Applicants respectfully remind the Examiner that a *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention. *In re Geisler*, 116 F.3d 1465, 1471, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997). In fact, teaching away from the art is a *per se* demonstration of lack of *prima facie* obviousness. *In re Dow Chemical Co.*, 837 F.2d 469, 5 U.S.P.Q.2d 1529 (Fed. Cir. 1988). Accordingly, it is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983); M.P.E.P. § 2145. The co-planar design of the Hakey reference cannot be maintained if the die are stacked. Because the Hakey reference actually teaches away from combining it with the Pai reference, the references cannot possibly be combined to render the recited subject matter obvious.

With regard to Moden, the Moden reference discloses a package comprising a semiconductor die 12 coupled to an adapter board 18 which is then coupled to a master board 30. Col. 4, lines 13-32. As explicitly stated in the Moden reference, the "adapter board" is a printed circuit board or substrate. Col. 3, lines 7-10. Applicants assume that the Examiner is applying the semiconductor die 12 and the adapter board 18 of the Moden reference to illustrate a die stack "wherein each die in the stack of at least 2 die is successively thinner than the previous die." However, it is clear that the Moden reference only discloses a package having a single semiconductor die 12. It is clear that the adapter board 18 disclosed in the Moden reference is *not* a semiconductor die. Therefore, the thickness of the adapter board 18 is irrelevant. The

Moden reference does not disclose a stack of successively thinner die. For at least this reason, neither the Hakey reference nor the Moden reference, taken alone or in combination discloses each of the elements recited in claims 68, 69 and 70, much less provides any suggestion to combine these references in the manner recited in the present claims. Accordingly, the cited combination cannot possibly render the recited subject matter obvious.

For at least the reasons set forth above, Applicants respectfully submit that claims 68-70, as well as those claims dependent thereon, are not rendered obvious by the cited combination. Thus, the Examiner's rejection of independent claims 68-70, as well as those claims dependent thereon, is improper. Accordingly, Applicants respectfully request that the Examiner withdraw the rejection and allow claims 68-70, as well as those claims dependent thereon.

In addition to the arguments set forth above, Applicants submit that the rejection of independent claim 68 is improper for an additional reason, as well. As with claims 35 and 38, claim 68 additionally recites an integrated circuit comprising a die stack coupled to a substrate, "each of the semiconductor die being coupled together by a first adhesive, the first adhesive being curable at a first temperature," and wherein the stack is coupled to a substrate by a second adhesive, "the second adhesive being curable at a second temperature lower than the first temperature."

In rejecting claims 68, the Examiner stated:

> (it is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight. Even though product-

by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patentability of a product does not depend on its method of production." MPEP 2113)

Office Action, page 10.

As discussed above with regard to claims 35 and 38, while Applicants agree with the Examiner's statement regarding the patentable weight of process limitations in a product-by-process claim, Applicants respectfully traverse the Examiner's assertion that claim 68 is in fact a product-by-process claim. As stated above, claim 68 recites a first adhesive "being *curable* at a first temperature," and a second adhesive "being *curable* at a second temperature lower than the first temperature." (Emphasis added). The present claim does not recite an actual act of curing the adhesive. In contrast, the present claim recites physical qualities of each of the first and second adhesives. That is, the first adhesive is "curable at a first temperature," and the second adhesive is "curable at a second temperature." For instance, the first adhesive used in the die stack may have properties such that it is curable at a high temperature, such as in the range of 50-400° C, for example. Page 12, lines 8-9. The adhesive used to attach each die together may be different than the adhesive which may be used later to attach the die to the substrate. Page 12, lines 12-14. The second adhesive may be curable at a second temperature such as in the range of 50-100° C, for example. As will be appreciated by those skilled in the art, in order for the adhesives to be curable at different temperatures, the adhesives have different physical qualities. Accordingly, Applicants respectfully submit that these structural limitations should indeed be given patentable weight.

Applicants respectfully submit that the Examiner's failure to give patentable weight to these structural limitations was improper. For this additional reason, Applicants respectfully

request that the Examiner withdraw the rejection and allow claim 68, as well as those claims dependent thereon.

Conclusion

In view of the remarks set forth above, Applicants respectfully request withdrawal of the Examiner's rejections and allowance of claims 35, 37-39, 45, 47-49, 63, and 65-70. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

General Authorization for Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefore. Furthermore, Applicants authorize the Commissioner to charge the appropriate fee for any extension of time to Deposit Account No. 13-3092; Order No. MICS:0078-1/FLE (01-0752.01).

Respectfully submitted,

Date: October 13, 2005

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